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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,283	01/08/2001	Brian Wyld	50990019US	4661

7590 05/09/2005

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EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,283	WYLD, BRIAN	
	Examiner	Art Unit	
	Joseph D. Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11, 13-17* is/are allowed.

6)☒ Claim(s) *9, 10, and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 9, 10, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Harper, U.S. Patent 6,675,316.

3. Referring to claim 9, Harper discloses multiple shared memory processor instances that communicate over an interconnection fabric, which is interpreted as a distributed multiprocessor system (See Fig. 1 and 4, and Col. 3, lines 13-14). The system has at least two hosts with a processor and internal memory (See Fig. 2). Harper also teaches the system having external memory nodes that are made reliable, "fault tolerant", (See Fig. 1 and 2, and Col. 4, lines 52-56), and the processors of the host have access to the L3 cache memory the via bus between the processors and a coherency control chipset as well as access to the external memory via the same bus, this is interpreted as a access device connected to the external memory unit through a

memory bus which is connected with the internal memory so that the access device provides the processing unit of the host with a transparent access to the external memory unit (See Fig. 2 and 4).

4. Referring to claim 10, Harper teaches the system having access to the external memory in the range of tens of nanoseconds (See Col. 5, lines 21-22). This is interpreted as the system having an access time to the external memory within three orders of magnitude than an access time to the internal memory.

5. Referring to claim 12, Harper discloses the processor and coherency control chipset connected via a bus (See Fig. 2), which is interpreted as the access device in the host connected to a bus. Harper teaches the system having access to the external memory in the range of tens of nanoseconds (See Col. 5, lines 21-22). This is interpreted as access to the external memory taking place in less than one cycle of the bus.

Allowable Subject Matter

6. Claims 11 and 13-17 are allowed.

Response to Arguments

7. Applicant's arguments, see page 5 of amendment, filed 24 January 2005, with respect to claims 13 and 14 have been fully considered and are persuasive. The objection of claims 13 and 14 has been withdrawn.

8. Applicant's arguments, see page 5 of amendment, filed 24 January 2005, with respect to claims 9, 11, and 12 have been fully considered but they are not persuasive. The applicant argues the cited prior art does not disclosure or suggestion of the external and internal memory units and the access device being connected to the same memory bus so as to provide the claimed transparent access. The examiner respectfully disagrees. Harper discloses the processors of the host have access to the L3 cache memory, internal memory, via the bus between the processors and a coherency control chipset as well as access to the external memory via the same bus (See Fig. 2 and 4), this is interpreted as processors have transparent access to both the internal and external memory. The above claims have been altered to clarify this and the previous rejection is maintained.

9. Applicant's arguments, see pages 5-7 of amendment, filed 24 January 2005, with respect to claims 15-17 have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejection of claims 15-17 has been withdrawn.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
May 3, 2005

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100